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06ES33

Third Semester B.E. Degree Examination, December 2010
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the definition of combinational logic. **(04 Marks)**

b. Simplify the function $y = f(a, b, c, d) = \Sigma\, m(2,3,4,5,13,15) + \Sigma\, d(8,9,10,11)$, using Karnaugh map. **(05 Marks)**

c. Simplify the function $y = f(a,b,c,d) = \pi M(0,4,5,7,8,9,11,12,13,15)$ using the Karnaugh map. **(05 Marks)**

d. Simplify the function $y = f(a,b,c,d,e) = \Sigma\, m(0,2,8,10,16,18,24,26)$ using the Karnaugh map. **(06 Marks)**

2 a. Simplify using the Quine-McClusky minimization technique $y = f(a,b,c,d) = \Sigma\, m(0,2,8,10)$. **(10 Marks)**

b. Simplify using the variable entered method (VEM),
$y = f(a,b,c,d,e) = \Sigma\, m(1,3,4,6,9,11,12,14,17,19,20,22,25,27,28,30) + \Sigma\, d(8,10,24,26)$. **(10 Marks)**

3 a. Perform the following to design a combinational logic circuit to convert the BCD digit to an excess – 3 BCD digit.
i) Construct the truth table, ii) write the min term equation for each output function, iii) Simplify the output function and write reduced logic equation and iv) Draw the resulting logic diagram. **(10 Marks)**

b. Draw the logic diagram for 2-to-4 logic decoder, with an active low encoder enable and active high data outputs. Construct a truth table and identify the data inputs, the enable input and the outputs. Describe the circuit function. Draw the logic symbol for decoder. **(10 Marks)**

4 a. Perform the following to design a full-subtractor:
i) Construct the truth table and simplify the output equations. ii) Draw the resulting logic diagram and iii) Realize the subtractor, using a decoder. **(10 Marks)**

b. Write a true table for two-bit magnitude comparator. Write the Karnaugh map for each output of two-bit magnitude comparator and the resulting equation. **(10 Marks)**

PART – B

5 a. What is the difference between a flip-flop and a latch? What is the gated SR latch? Explain the operation of gated SR latch, with a logic diagram, truth table and logic symbol. **(10 Marks)**

b. Explain the operation of positive-edge-triggered JK flip-flop and T flip-flop, with the help of logic diagram, function table and logic symbol. **(10 Marks)**

6 a. Explain the working principle of four-bit binary ripple counter, with the help of a logic diagram, timing diagram and counting sequence. **(10 Marks)**

b. Explain the design of a synchronous Mod-6 counter, using the clocked flip-flops. Clearly indicate the application table, excitation table and minimal sum expressions. **(10 Marks)**

7 a. Draw the Mealy and Moore synchronous machine models. Label the excitation variables, state variables, input variables and output variables, in both the diagrams. **(08 Marks)**

b. For the logic diagram given in Fig.Q7(b),

i) Derive the excitation and output equations,

ii) Write the next state equations,

iii) Construct a transition table and

iv) Draw the state diagram. **(12 Marks)**

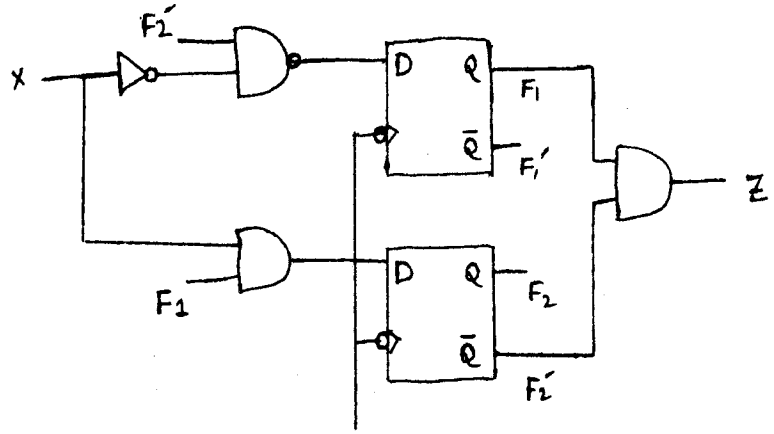

Fig.Q7(b)

8 Design a cyclic module-8 synchronous binary counter, using JK flip-flops, to count the number of occurrences of an input, i.e., the number of times it is a 1. The input variable x must be coincident with the clock to be counted. The counter is to count in binary. The design should clearly indicate the following :

a. State diagram and state table. **(05 Marks)**

b. Transition table and excitation table. **(05 Marks)**

c. Karnaugh maps **(05 Marks)**

d. Logic diagram. **(05 Marks)**

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